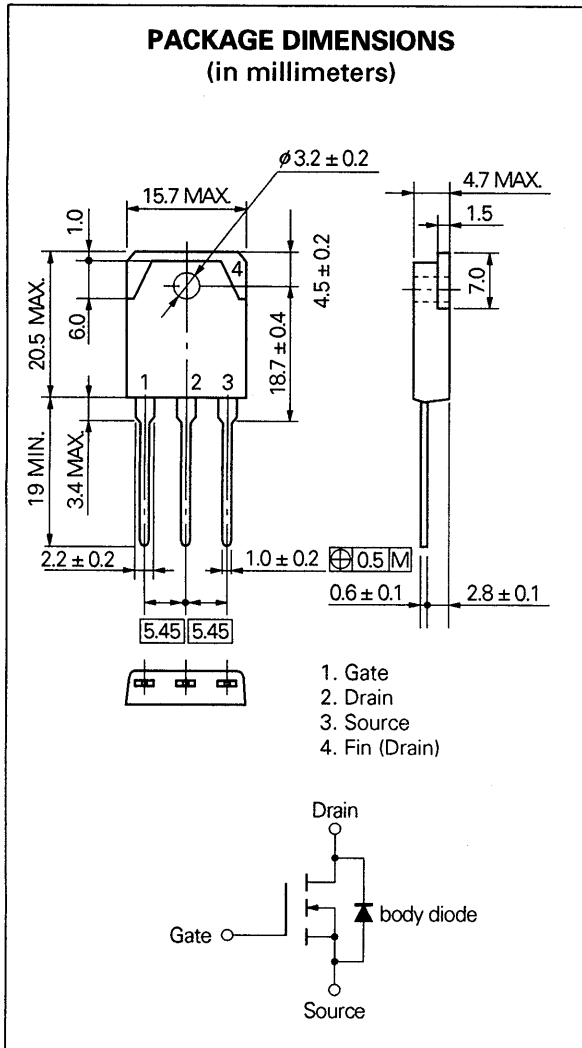


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P1 98.2

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE



DESCRIPTION

The 2SK1271 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- High Voltage Rating $V_{DS} = 1\ 400\ V$
- Low On-state Resistance
 $R_{DS(on)} = 4.0\ \Omega\ MAX.$ ($V_{GS} = 10\ V, I_D = 3\ A$)
- Low C_{iss} $C_{iss} = 1\ 800\ pF\ TYP.$

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	-55 to +150 °C
Channel Temperature	150 MAX. °C

Maximum Power Dissipation

Total Power Dissipation ($T_c = 25\ ^\circ C$)	240	W
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Maximum Voltages and Currents ($T_a = 25\ ^\circ C$)

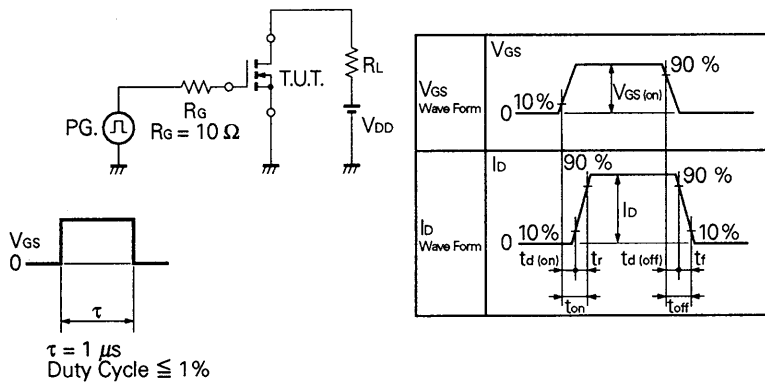
V_{DS}	Drain to Source Voltage	1 400	V
V_{GS}	Gate to Source Voltage	± 20	V
$I_{D(DC)}$	Drain Current (DC)	± 5	A
$I_{D(pulse)*}$	Drain Current (pulse)	± 10	A

* $PW \leq 10\ \mu s, Duty\ Cycle \leq 1\ %$

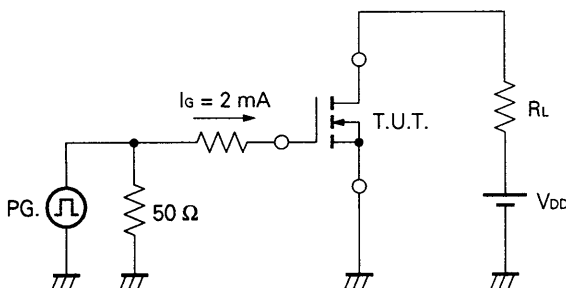
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		3.5	4.0	Ω	V _{GS} = 10 V, I _D = 3 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	1.5			S	V _{DS} = 20 V, I _D = 3 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = 1 120 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±100	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		1 800		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		500		pF	
Reverse Transfer Capacitance	C _{res}		360		pF	
Turn-On Delay Time	t _{d(on)}		25		ns	V _{GS} = 10 V V _{DD} = 150 V I _D = 3 A, R _G = 10 Ω R _L = 50 Ω
Rise Time	t _r		30		ns	
Turn-Off Delay Time	t _{d(off)}		220		ns	
Fall Time	t _f		40		ns	
Total Gate Charge	Q _G		125		nC	V _{GS} = 10 V I _D = 5 A V _{DD} = 450 V
Gate to Source Charge	Q _{GS}		15		nC	
Gate to Drain Charge	Q _{GD}		70		nC	
Diode Forward Voltage	V _{F(S-D)}		0.9		V	I _F = 5 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		1 400		ns	I _F = 5 A di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		30		μC	

Test Circuit 1: Switching Time

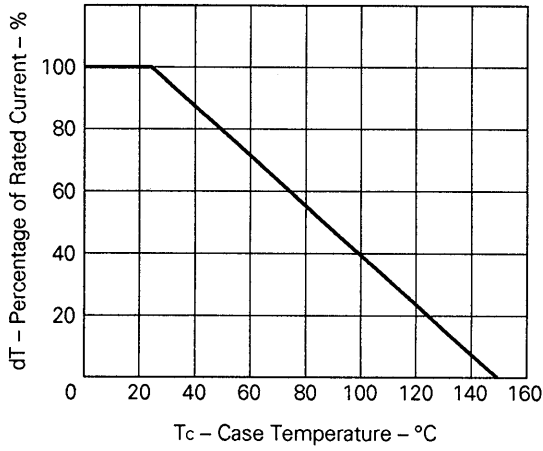


Test Circuit 2: Gate Charge

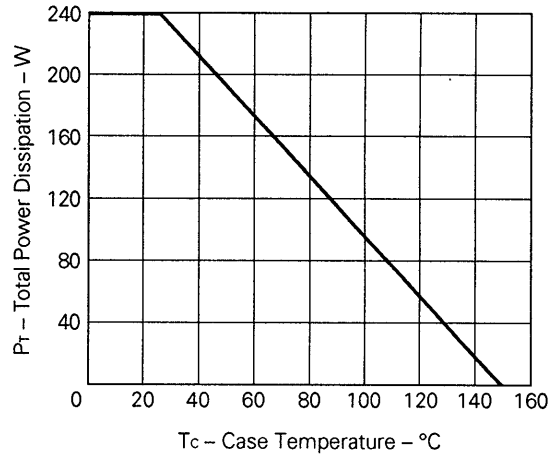


TYPICAL CHARACTERISTICS (T_a = 25 °C)

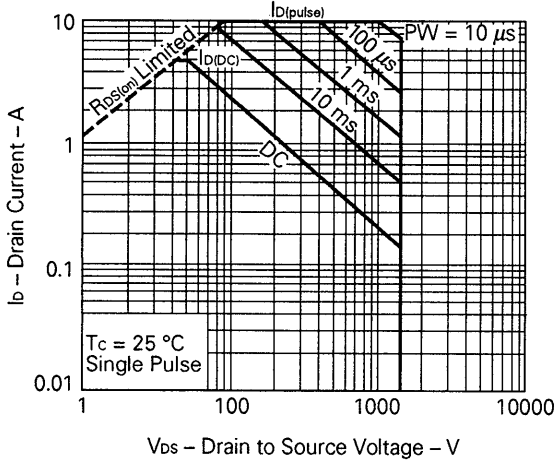
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



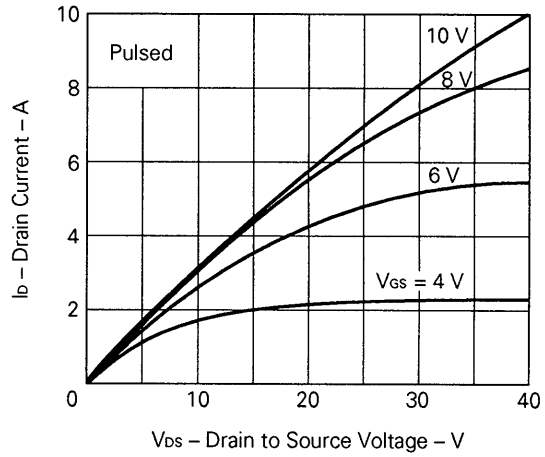
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



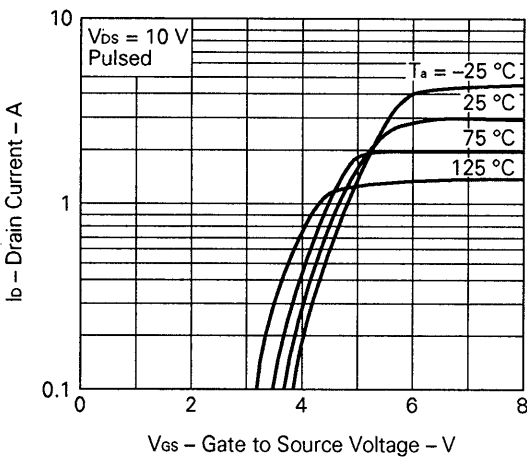
FORWARD BIAS SAFE OPERATING AREA



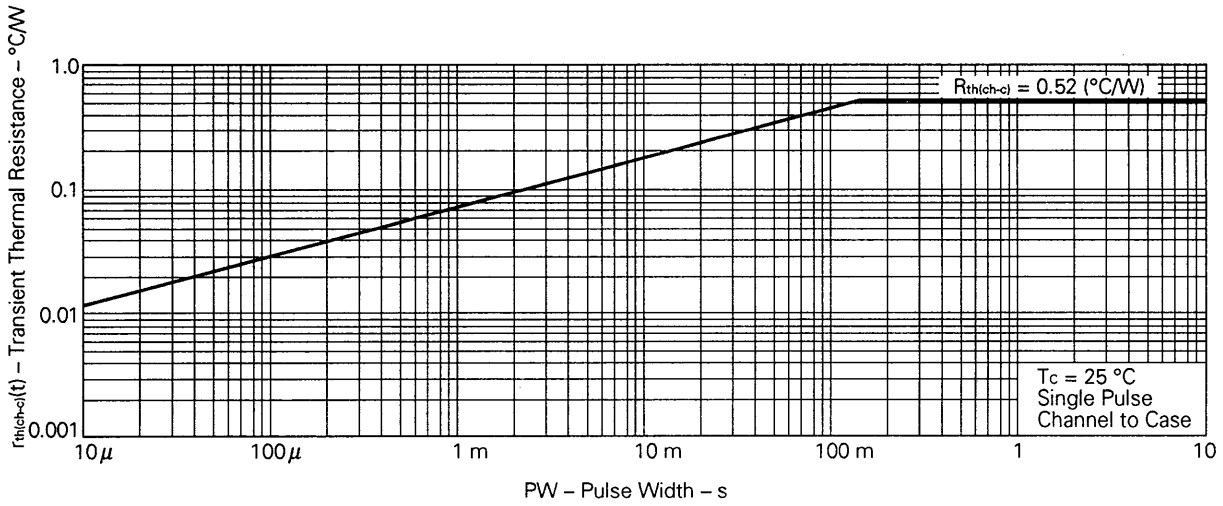
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



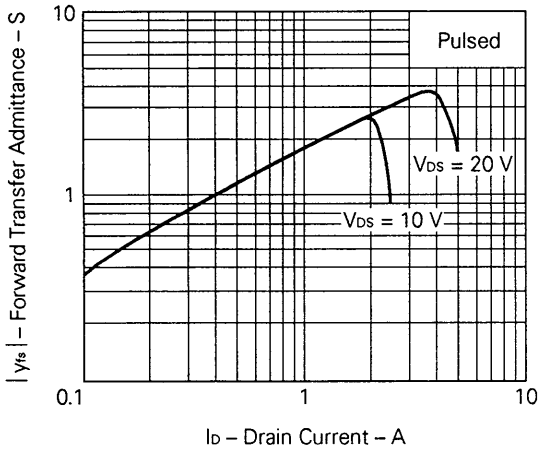
TRANSFER CHARACTERISTICS



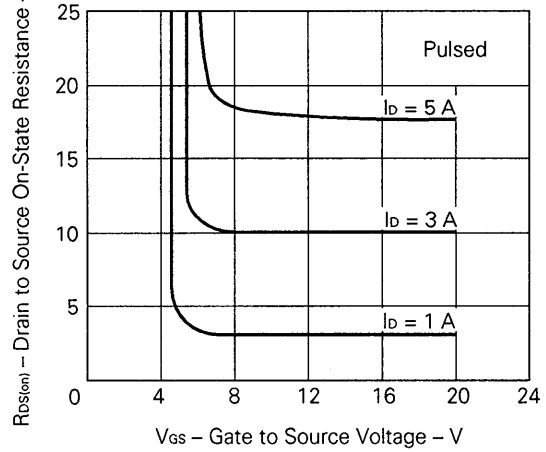
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



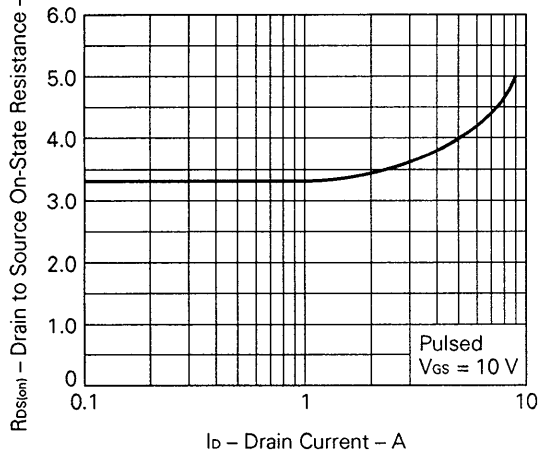
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



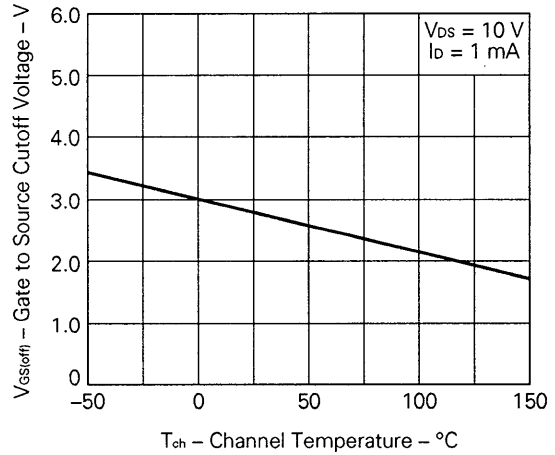
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

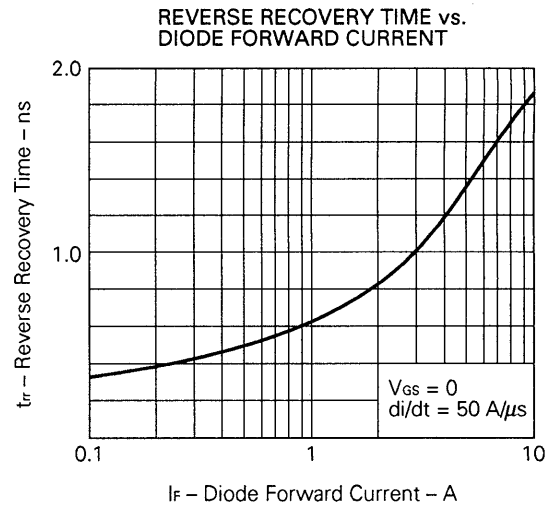
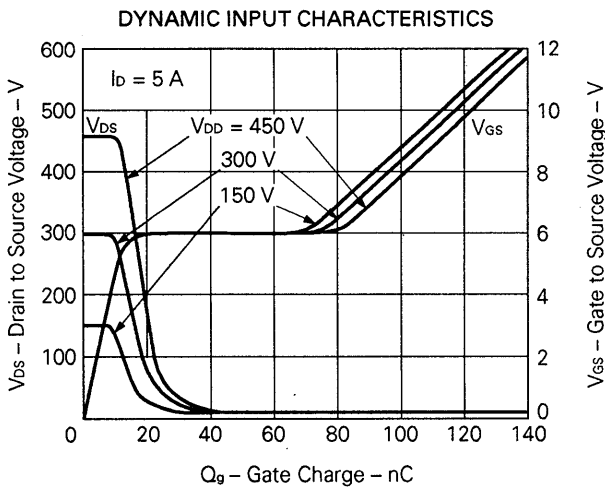
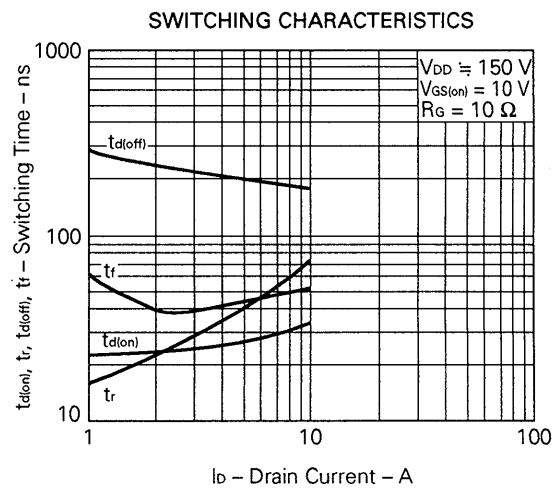
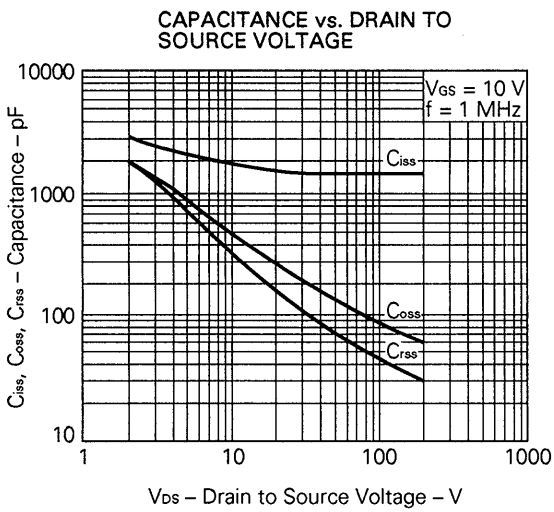
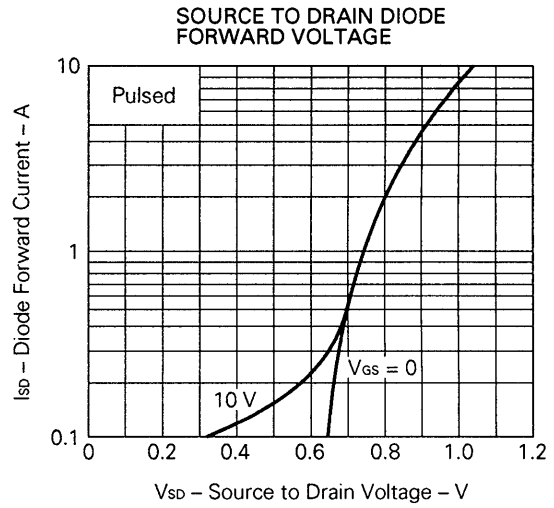
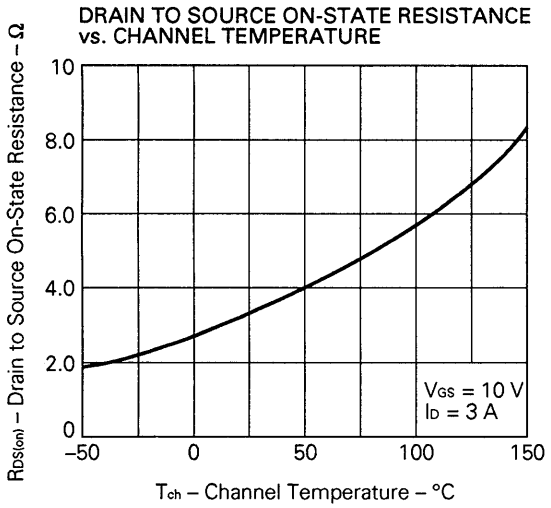


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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